

**OnChip Systems****SAM8905****digital sound generator/processor for musical applications****GENERAL DESCRIPTION**

The SAM8905 is a general purpose digital sound generator/processor designed for audio requirements. Its very flexible features makes it an ideal circuit for use in a variety of musical products such as keyboards, synthesizers, organs, rhythm units, samplers, workstations, expanders, electronic pianos, home computer add-on,...

FEATURES

- CD quality audio generation : stereo 16 bits output, 44.1 kHz sampling rate
- User definable synthesis modes : algorithms down-load into built-in RAM
- Polyphonic 16 voices, polytimbral 8 sounds
- High performance : sinus operator 176.8 ns, FM operator 265.2 ns, 2nd order filter 663 ns
- Built-in 4k x 12 sinus table and ramp
- 1 Mega x 12 of external sampling memory directly addressable, any size with paging
- Stereo mix (pan and volume) independent for each sound component
- 19 bits internal data path, 24 bits accumulate with clipping circuitry
- Directly compatible with popular compact disc serial DACs : TDA1541, TD1543, AD1856
- Compatible with popular oversampling digital filter chips used in digital audio
- Single supply low-power HCMOS, 68 pins PLCC

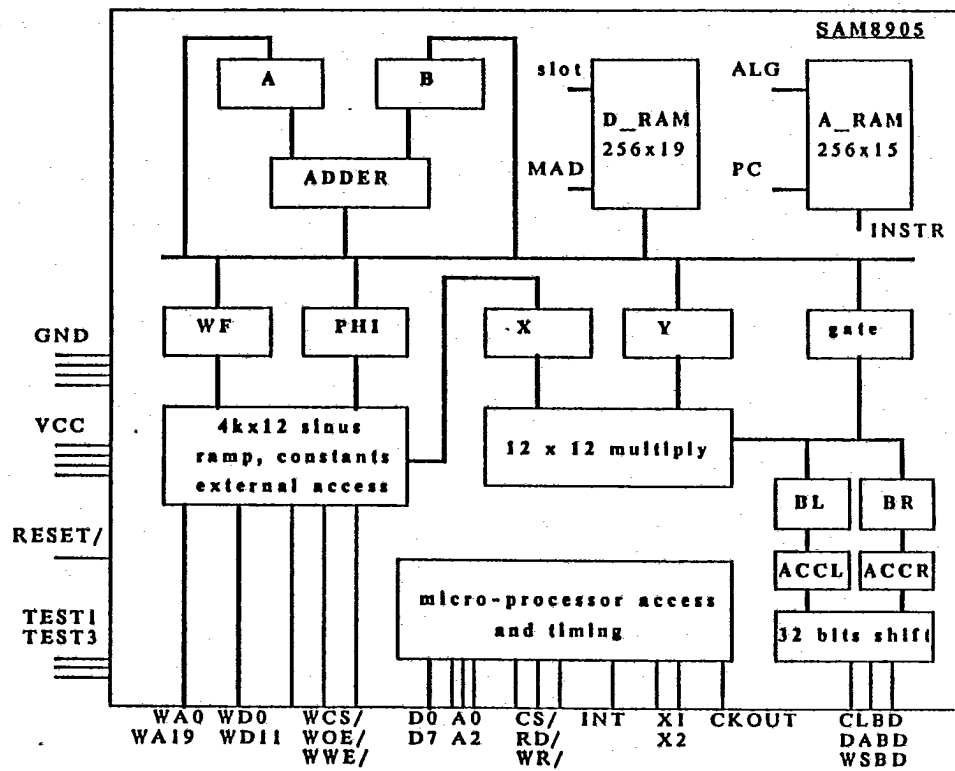


Fig 1 - Block diagram

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sam8905 data sheet

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1- General description

The SAM8905 is organized around an internal 19 bits data bus. Following elements are connected to this bus :

- **Adder block** : A register (19 bits), B register (19 bits) and 19 bits two's complement adder. Specific micro-instructions allow to write the bus to the A and/or B register and read the result of the A+B addition back to the bus. It is also possible to conditionnaly write to the A register.

- **D_RAM** : This 256 x 19 RAM is divided into 16 blocks of 16 words. A block is selected by a slot number, while a word inside a block is defined in the micro-instruction. The D_RAM holds algorithm parameters, like frequency, phase, amplitudes, sampling memory address. The D_RAM can be accessed (read/write) by the external micro-processor and it can be read, written, and conditionnaly written under control of the micro-program. Word 15 of each D_RAM block also holds specific information concerning the algorithm number associated to the slot and its status.

- **WF (9 bits) and PHI (12 bits) registers** : WF together with PHI specifies a full 20 bit address for sampling. Specific WF values allow to select the internal sinus ramp or constant.

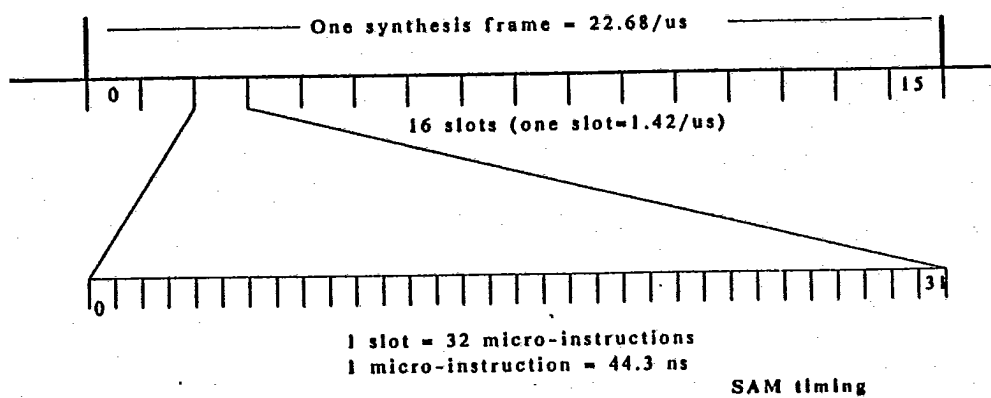
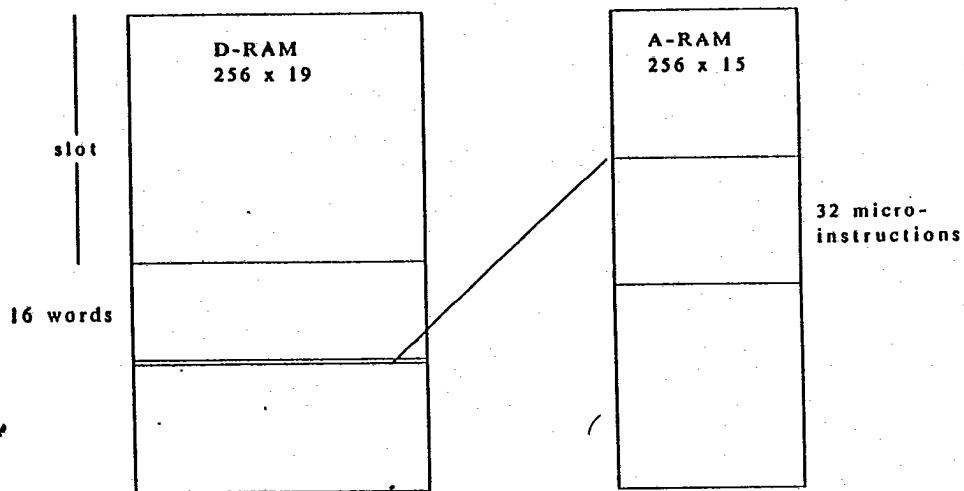
- **Multiplier block** : X register (12 bits), Y register (12 bits) and 12 x 12 two's complement multiplier. X holds the sample data and Y receives from the bus a coefficient (normally an amplitude) to be applied to this sample. The 12 x 12 multiplier gives a 23 bits signed result which is rounded into 19 bits. The result X x Y can be read back to bus by the "gate", or accumulated into the left and right 24 bits accumulators (ACCL, ACCR), after attenuation through the BL and BR barrel shifters. Every frame of synthesis (typ. 22.68 /us), the content of the accumulators is transferred to a 32 bits shift register and the accumulators are cleared. The accumulators also include a clipping circuitry to prevent digital overflow.

- **A_RAM** : This 256 x 15 RAM is divided into 8 blocks or 32 words or 4 blocks of 64 words. Each block holds a specific algorithm, which is a sequence of micro-instructions. The A_RAM can be accessed (read/write) by the external processor. A new micro-instruction (INSTR) is processed every cycle (typ. 44.3 ns).

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SAM Memory structure

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2- Overview of operation

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This overview assumes SSR=0 in the SAM control word.

Each frame of synthesis (typ 22.68 /us), new left and right data are transferred to the external DAC, while new data is being processed and accumulated into the left and right accumulators (ACCL, ACCR).

Each frame of synthesis is divided into 16 time slots, each slot being further divided into 32 micro-instructions. The 16 D_RAM blocks are sequentially accessed by slot number, the first action at the beginning of a new slot is to select which algorithm is assigned to the slot, by reading word 15 of the new slot.

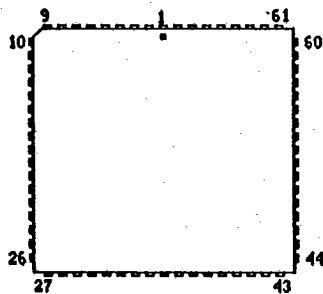
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Pin-out :

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1- GND	18- GND	35- GND	52- GND
2- WA16	19- D6	36- X2	53- WA3
3- WA15	20- D7	37- DABD	54- WD7
4- WWE/	21- CS/	38- CLBD	55- WA4
5- WA17	22- A0	39- WSBD	56- WCS/
6- WA18	23- A1	40- WD11	57- WA5
7- WA19	24- A2	41- WD10	58- WA13
8- WA0	25- INT	42- WD9	59- WA6
9- WA1	26- WR/	43- WD8	60- WOE/
10- VCC	27- VCC	44- VCC	61- VCC
11- WA2	28- RD/	45- WD3	62- WA7
12- D0	29- TEST1	46- WD2	63- WA14
13- D1	30- TEST2	47- WD4	64- WA8
14- D2	31- TEST3	48- WD1	65- WA12
15- D3	32- RESET/	49- WD5	66- WA9
16- D4	33- CKOUT	50- WD0	67- WA11
17- D5	34- X1	51- WD6	68- WA10



68 pins PLCC

Fig 3 - Pin-out

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3- Pin description

GND	1,18,35,52	IN	Power ground, all these pins should be returned to ground.
VCC	10,27,44,61	IN	+5V supply, all these pins should be returned to +5V
D0-D7	12-20	IN/OUT	8 bits data bus to/from micro-processor
A0-A2	22-24	IN	Address select from micro-processor. A2=0 selects 1 out of 4 data registers for read or write, A2=1 selects the control register for write.
CS/	21	IN	Chip select, active low
RD/	28	IN	Read chip interrupt status/data from /uP, active low
WR/	26	IN	Write control/data to chip from /uP, active low
INT	25	OUT	Interrupt request to micro-processor, active high
X1	34	IN	Xtal or external clock (45.1584 MHz for CD 44.1 kHz)
X2	36	OUT	Other Xtal connexion, leave open if external clock is used.
CKOUT	33	OUT	Output clock (Xtal divided by 4, typ=11.2896 Mhz), used to drive an external micro-processor.
RESET/	32	IN	Chip reset . Sets idle mode in control register. This signal should be held low for at least 10 ms after power up
DABD	37	OUT	Serial data out to external DAC
CLBD	38	OUT	Clock to external DAC
WSBD	39	OUT	Left/Right channel select to external DAC
WA0-WA19	2-11 53-68	OUT	External sampling wave memory address.
WD0-WD11	40-54	IN/OUT	External sampling wave memory data.
WCS/	56	OUT	External sampling wave memory chip select, active low
WOE/	60	OUT	External sampling wave memory output enable. Used when the wave memory is RAM, to allow write operation, active low.
WWE/	4	OUT	External sampling wave memory write, active low
TEST1 -TEST3	29-31	IN	Test pins, should be returned to VCC

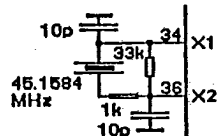
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4- Oscillator characteristics

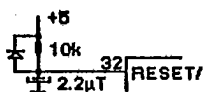
Depending on the type of quartz used (fundamental, 3rd overtone), on the quality factor and on stray capacitance, it may be necessary to compensate the quartz with serial/parallel resistors and compensation capacitors (see figure, values are indicative and may vary from design to design). The quartz frequency is 1024 times the sampling frequency with SSR=0 (typ. 45.1584 MHz for 44.1 kHz sampling freq). An external clock can be connected to pin X1 (CMOS level). In this case X2 should be left open. A bad quartz compensation or PC board lay-out will result in missing oscillator pulses and consequently memory errors inside the circuit.

Typical quartz connection :



5- Power-up reset

The RESET/ signal should be held low until the quartz oscillator is stabilized. The best solution is to use the generated reset signal from an external micro-processor. If such a signal is not available, then following circuitry could be used :



6- ABSOLUTE MAXIMUM RATINGS*

Ambient temperature under bias	0°C to +70°C
Storage temperature....	-65°C to +150°C
Voltage on any pin to GND.....	-0.5V to VCC+0.5V
Voltage on VCC to GND....	-0.5V to 6.5V
Maximum IOL per I/O pin....	10 mA

*Notice: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and operation of the device is not implied.

WARNING : ESD sensitive device. Observe precautions for handling.

7- D.C. CHARACTERISTICS (Ta=0°C to 70°C, VCC=5V +/- 10%)

Symbol	Parameter	min	typ	max	unit	test conditions
Vil	Input low voltage	-0.5		0.8	V	
Vih	Input high voltage	2.0		VCC+0.5	V	
Vol	output low voltage			0.45	V	Iol=3.3 mA
Voh	output high voltage	2.4			V	Ioh=-0.8 mA
Icc	power supply current		10	25	mA	quartz=45.1584 MHz

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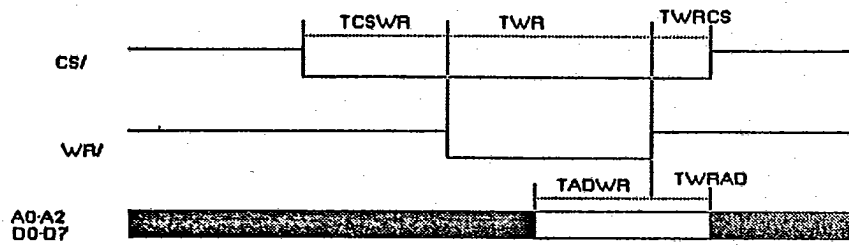


Fig 4 - Processor Write cycle

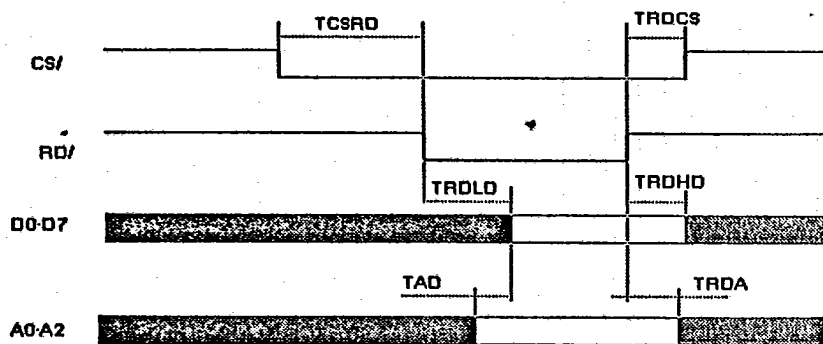


Fig 5 - Processor read cycle

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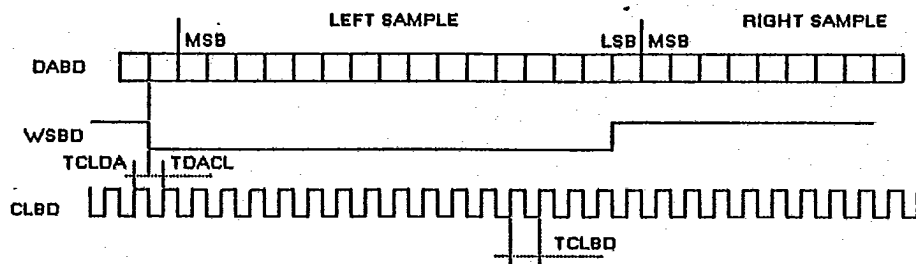


Fig 6 - External DAC timing

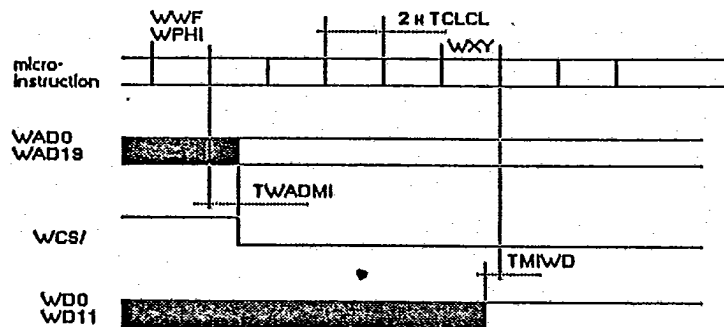


Fig 7 - external memory read

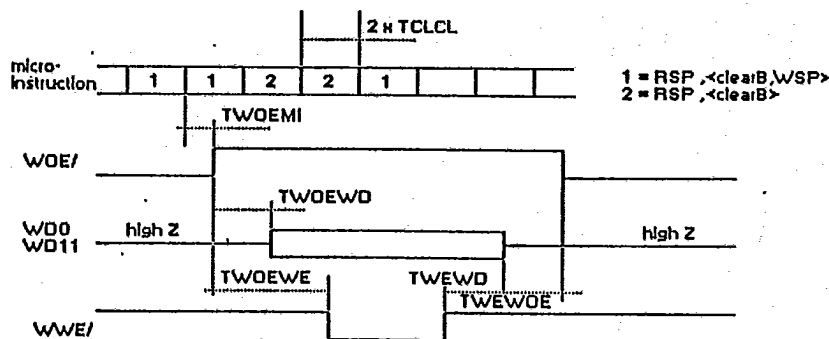


Fig 8 - External memory write

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8- A.C. CHARACTERISTICS

(Ta=0°C to 70°C, VCC=5V +/- 10%, load capacitance=80pF for all outputs except X2)

Symbol	Parameter	min	typ	max	unit
I/TOLCL	oscillator frequency	0		48.1584	MHz
TCSWR	CS/ low to WR/ low	50			ns
TWRCS	WR/ high to CS/ high	20			ns
TADWR	A0-A3, D0-D7 valid to rising WR/	20			ns
TWRAD	A0-A3, D0-D7 valid after rising WR/	10			ns
TWR	WR pulse width	50			ns
TCSRd	CS/ low to RD/ low	50			ns
TRDCS	RD/ high to CS/ high	20			ns
TRDLd	RD/ active to valid data out		50		ns
TRDHD	data out hold from RD/	10			ns
TAD	A0-A3 valid to valid data out		50		ns
TRDA	A0-A3 hold from RD/	10			ns
Trecover	recover from control write	32 x TOLCL+10			ns
TCLBD	CLBD period		32 x TOLCL		
TDACL	DABD/WSBD stable to rising CLBD	16 x TOLCL-10			ns
TCLDA	DABD/WSBD stable after rising CLBD	16 x TOLCL-10			ns
TWADM	WAD0-10 valid from WWF or WPHI micro-instruction		10		ns
TMIWD	WD0-11 valid before WXY micro-instruction	10			ns
TWOEMI	WOE/ high from RSP clearB micro-instruction		10		ns
TWOEWD	WD0-11 out valid (Y register) from WOE/ high		TOLCL		ns
TWOEWE	WWE/ low from WOE/ high		2 x TOLCL		ns
TWEWD	WWE/ high to WD0-11 high Z		TOLCL		ns
TWEWOE	WWE/ high to WOE/ low		TOLCL		ns

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sam8905 programmers's guide

1- Purpose

This section describes how to use the SAM chip from a software programmer point of view.

2- Introduction

The SAM is a powerful signal processor oriented towards music. It generates sound by computing the samples in an "algorithm", which is a succession of micro-instructions.

The SAM is not predefined for any particular synthesis : the algorithms are stored in a built-in RAM, which has to be loaded at power-up by the main processor. This makes it very flexible to adapt to different products. Furthermore, algorithms can be loaded while the synthesis is in progress.

The SAM has a built-in sinus/ramp generator. However, for application involving sampling, up to 1 M words of 12 bits sampling memory (RAM or ROM) can be directly connected. With a few external circuits, up to 256 mega words of DRAM sampling memory can be connected (ref : application note, using the SAM with dynamic RAMs).

Using the SAM involves :

1- Defining and coding the algorithms :

For this purpose a language, a compiler and a "code view" debugger are available, as part of a whole package for product development.

2- Controlling the SAM in a real time environment :

- Algorithms down-loading
- Algorithms parameters control

3- SAM basic operation

The following assumes that the SAM is used with a 45.1584 MHz quartz.

The SAM can operate at two different sampling rates : 44.1 kHz (CD standard) or 22.05 kHz. The choice of the sampling rate has to be done when defining the product as it greatly influences algorithm sizes, number of simultaneous algorithms, polyphony and sound quality. In the following, we will assume that the 44.1 kHz sampling rate is used, brackets [] will be used for the corresponding 22.05 kHz figures.

The SAM has two built-in RAMs : The micro-program RAM, referred as A-RAM (256 x 15), which holds the algorithms code and the parameter RAM, referred as D-RAM (256 x 19) which holds the algorithms parameters.

The A-RAM is divided into 8 [4] blocks, each block storing a single algorithm of 32 [64] micro-instructions.

The D-RAM is divided into 16 blocks of 16 words (19bits width), each block holding the parameters of a specific algorithm. The algorithm number related to a particular block is stored at address 15 of the block.

The 44.1 kHz [22.05 kHz] sampling rate corresponds to a time of 22.68 /us [45.35 /us], known as a "frame".

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The "frame" is divided into 16 "slots", each slot addressing sequentially one block of the D-RAM.

Each slot is divided into 32 [64] cycles, one micro-instruction from an algorithm being executed each cycle.

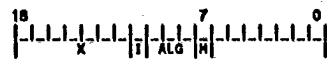
A micro-program starts at address 0 in each slot, addresses 30 and 31 [62 and 63] are reserved for micro-processor access and algorithm change and the corresponding micro-instructions are not processed.

A micro-program accumulates results of computations into a left channel and a right channel accumulator. At the end of a frame, the content of the accumulators is transferred to a final shift register. This shift register is directly compatible with a standard 16 bits stereo serial DAC.

4- Parameter RAM (D-RAM) format

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Any of the 16 x 19 bits words of a D-RAM block can be addressed during a slot by the micro-program. Only address 15 of a D-RAM should hold a specific information, as follows:

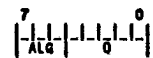


X : free for other information

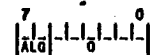
M : Interrupt mask, when set, this slot will not generate interrupts.

I : Idle, when set, this slot will execute a no-op algorithm, independently of the selected algorithm.

ALG: selected algorithm, will select the block in the A-RAM. Execution of the corresponding algorithm will start at address:



44.1 kHz sampling

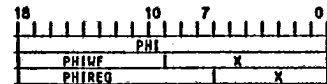


22.05 kHz sampling

Note : For 22.05 kHz sampling, only the 2 upper ALG bits are used to select the algorithm.

The other addresses of the D-RAM are not assigned to any specific information.

However, the word format of the D-RAM depends on the type of information, as follows :



Typical micro-instructions:
WA, WB, WPHI

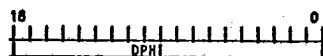
PHI : full phase of a period of a given waveform (unsigned integer)

PHIWF : Portion of phase recommended to access external waveforms (512 samples/period). Up to 12 bits can be used (4096 samples/period with the same frequency definition as the built-in sinus)

PHIREG: Portion of phase loaded at WPHI time, allows to address the internal 4096 samples/period sinus/ramp.

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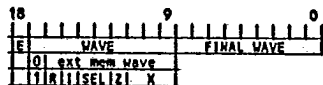
Typical micro-instructions :
WA, WB

DPHI : Phase interval, signed integer, determines the basic frequency of a signal as follows (standardized to the built-in sinus) :

$$f = 0.084114 \times \text{DPHI} \text{ (Hz)}$$

$$[f = 0.042057 \times \text{DPHI} \text{ (Hz)}]$$

Negative values of DPHI are mainly used for envelope applications (see later)



Typical micro-instructions :
WA WSP, WWP

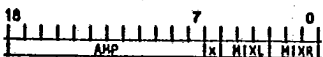
This format is mostly used in sampling applications, involving an external wave-form memory. Specific micro-instructions allow to selectively increment WAVE at the end of a period and to check if WAVE reaches FINALWAVE. Subsequent actions can be taken depending on the state of the E bit (END), like looping on a period or stopping the sampling process.

The upper bit of WAVE indicates an external (0) or internal (1) wave. For internal waves, the remaining bits have the following meaning :

- R : 0- Select sinus wave (internal $4k \times 12$ sinus). In this case the other bits should be zero.
1- Select ramp or constant
- I: 0- direct, 1- two's complement
- SEL: 00- 2 x PHI ramp
01- Constant from micro-instruction
10- PHI ramp
11- PHI/2 ramp
- Z: 1- select constant zero as waveform

See appendix I for more informations about sinus, ramps and constants.

When the upper bit of wave is 1, the remaining 8 bits, together with the 12 upper phase bits define the external sampling memory address.



Typical micro-instructions :
WXY, WXY WSP, WA, WB

This format allows to define an amplitude and an optional left and right mix. The amplitude is coded on 12 bits and ranges from -1 to $1-2^{-11}$.

MIXL and MIXR define the amount of signal to be send resp. to the left and right channels according to the following table :

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MIX/MIXR output attenuation

000	no signal to output
001	-36 dB
010	-30 dB
011	-24 dB
100	-18 dB
101	-12 dB
110	-6 dB
111	0 dB

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note : As the Mix is only updated by a WXY WSP, it can be handled in a very flexible way. The minimum requirement is to initialize this information.

5- Algorithm RAM (A-RAM) format

The philosophy of a micro instruction is to put one emitter of the bus in relationship with several receivers and/or modifiers and/or do a special action

The micro-instruction consists of 3 fields :

Emitter MAD , < Receiver0,receiver1,... ,modifier, special action>

The emitter field allows information to drive the internal 19 bits bus. Obviously, only one emitter can be active at a time. Emitters are defined with an "R" like "read". Possible emitters are the adder (RADD), the D-RAM (RM MAD), the multiplier output (RP), and "nothing" (RSP), which will leave the bus indeterminate but is used to write to the external memory (see later).

The MAD field allows to select the address (0 to 15) of the D-RAM into the current block. This field is blank if no D-RAM operation is involved (Don't forget the coma in this case).

The receiver /modifier/special action field:

A receiver stores the information of the 19 bits internal bus. Several receivers can be active at a time. Receivers are defined with a "W" like "write". Possible receivers are the A register (WA), the B register (WB), the D-RAM (WM), the phase register (WPHI), the X and Y registers (WXY) and the wave-form register (WWF).

The Modifier (WSP), modifies a receiver action.

The special actions as clearB which sets the B register to zero and WACC which accumulates the product into the left and right accumulators through the attenuators.

The general micro-instruction format is then :

```
[ RM      ]
[ RADD    ]      [ MAD ] , <[WA] [WB] [WM] [WFI] [WPHI] [WXY] [clearB] [WACC] [WSP] >
[ RP      ]
[ RSP     ]
```

RM and WM are exclusive

The WSP field, when present, will modify some receiver actions as follows :

WPHI WSP

The PHI register is loaded normally, but the WF register is set to 100H, which will select the sinus internal wave-form.

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WXY WSP

The X and Y registers are loaded normally, but the MIXL and MIXR fields of the bus are also loaded into the respective output attenuators.

WA WSP and WM WSP will be described later in detail.

6- Timing constraints

Normally, the result of an operation is available on the cycle following the loading of the operands. For example, the operation :

```
RM PHI, <WA>
```

can be immediately followed by

```
RADD ,<WPHI>
```

The result of the addition A+B being available one cycle after the A and B operands have been loaded.

Exceptions are :

- 1- Availability of the product (WXY to RP) : 2 cycles
- 2- Availability of the product for Accumulation (WXY to WACC) : 3 cycles
- 3- Availability of the wave sample (WWF or WPHI to WXY) :
 - 1- Internal ramp or constant : 1 cycle
 - 2- Internal sinus : 2 cycles
 - 3- External wave memory : $(t_{acc} + 44.2)/44.2$ cycles, t_{acc} being the access time of the external memory. For example, assume a 250ns access time memory, then 7 cycles are needed.

7- Simple algorithm examples

Example 1 : sinus oscillator

```

PHI=0      ;assign phase to address 0 of RAM block
DPHI=1     ;assign phase angle (frequency) to address 1
AMP=2      ;assign amplitude and mix to address 2 (see format under §4)

RM PHI, <WA,WPHI,WSP> ;Areg=PHIreg=D-RAM(PHI) Wfreq=100H (sinus)
RM DPHI, <WB>          ;Breg=D-RAM(DPHI)
RM AMP, <WXY,WSP>      ;X=sin(PHI) Y=AMP mix updated
RADD PHI, <WM>          ;D-RAM(PHI)= Areg + Breg (PHI+DPHI)
RSP        ;NOP to wait 3 cycles from WXY
RSP        ;<WACC>          ;accumulate AMP x sin(PHI) through mix
FIN        ;This statement will fill the rest of the algorithm with no-ops until the requested
           ;size (32 or 64) as defined by parameter SIZE

```

Example 2 : external memory wave oscillator (250 ns access time)

```

PHI=0      ;assign phase to address 0
WF=1       ;assign wave to address 1 (see format under §4), E and final wave are
           ;don't care
DPHI=2     ;assign phase angle to address 2
AMP=3      ;assign AMP and mix to address 3 (see format under §4)

RM WF, <WWF>          ;Wfreq=Wave select
RM PHI, <WA,WPHI>      ;Areg=PHIreg=D-RAM(PHI)
RSP        ;nops to ensure 7 cycles from WPHI to WXY
RSP
RSP
RSP
RSP
RM DPHI, <WB>          ;Breg=D-RAM(DPHI)
RADD PHI, <WM>          ;D-RAM(PHI)= Areg + Breg (PHI+DPHI)
RM AMP, <WXY,WSP>      ;X=wave(PHI) Y=AMP mix update
RSP        ;nop to wait multiplier result
RSP        ;nop to wait multiplier result
RSP        ;accumulate
FIN        ;fill with nops til size of algorithm

```

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notes: The nope area can in most cases be used to implement modulations or overlap with the next computation.

As it can be seen from the previous examples, a single algorithm can implement up to 7 [15] sinus oscillators, which means that the polyphony of the SAM is 112 [240] simple sinus oscillators. Also, the polyphony achieved when accessing external memory greatly depends upon the external memory access time. With the example given (250 ns access time), the wave polyphony is from 3 [7] for one algorithm, for a total SAM wave polyphony of 48 [112]. Using 100ns external memory will increase this polyphony to 80 [160]

With the SAM features described, one can implement all types of formulae synthesis, i.e. synthesis which can be defined with mathematical expressions involving multiply and add without limit conditions.

For example, the synthesis $S=A \sin(w_1 + M \sin w_2 t)$ is easily achieved (FM). Also possible are multiple FM, FM feedback, phase modulation, amplitude modulation, ring modulation, exponential envelope generation, digital filtering, etc. etc. A corresponding algorithm library is provided with the SAM toolkit. However, until now, synthesis invoking conditions, like sampling (loop when $WF=final\ WF$), MACROSampling™, formant synthesis (trigger a function with an excitation), envelope generation with a given envelope shape, etc. are not described. The purpose of the next chapter is to describe the SAM micro-instructions allowing such synthesis.

8- Micro-instructions for conditional synthesis : WA WSP and WM WSP

8-1- The CARRY from the A+B adder

The carry of the adder has a different meaning depending on the sign of the data in the B register :

- B register positive (bit 18 from Breg=0)

Then the CARRY is the normal carry of an addition (bit 19 of the result of the A+B addition in twos complement).

- B register negative (bit 18 from Breg=1)

Then the CARRY is the complement of the sign bit of the addition (complement of bit 18 of A+B).

Examples

A	B	CARRY	A+B (RADD)
1000H	2000H	0	3000H
7FFFFFFF	1	1	0
7FFFFFFF	7FFFFFFF	0	7FFFFFFE (-2)
40000H	7FFFFFFF	1	3FFFFFFF

This carry mechanism allows to deal with one half of a signal period.

8-2 The CLEARROST and INTMOD flip-flops

This flip-flops are updated by WA and WA WSP and are tested by WM WSP, allowing conditional write to the D-RAM and corresponding interrupt request.

8-3 The WA WSP micro-instruction

WA (without WSP) always sets the CLEARROST flip-flop and clears the INTMOD flip-flop.

WPHI WSP takes priority over WA WSP giving a normal WA

WA WSP expects an E|WAVE|final|WAVE format on the bus (see §4)

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WSP	CARRY	WF=finalWF	END	value loaded in A	CLEARRQST	INTMOD
no	X	X	X	19 bits bus	1	0
yes	0	X	X	00000H	0	1
yes	1	no	X	00200H	0	1
yes	1	yes	0	00000H	0	1
yes	1	yes	1	00000H	1	1

8-4 The WM WSP micro-instruction

This micro-instruction allows to conditionally write to the D-RAM, according to CLEARRQST and CARRY. Also, an interrupt may be requested to the external processor, assuming that the interrupt mask bit at D-RAM address 15 is reset (see §4).

CLEARRQST	CARRY	INTMOD	write bus to D-RAM	Request interrupt
no	X	X	no	no
yes	0	0	yes	no
yes	0	1	yes	yes
yes	1	X	no	yes

8-5 Using WA WSP and WM WSP**8-5-1 Increment of the waveform number at the end of a period**

This is used mainly for sampling, but can find other applications like slow linear ramps, etc. The following example assumes a 200 ns external sampling memory

```

PHI=0      ;period phase
WF=1       ;initial and final sampling periods, E should be set if the AMP should
           ;drop to 0 when WAVE=finalWAVE (see §4 for format)
DPHI=2     ;frequency
AMP=3      ;amplitude and mix

RM         WF,      <WAVE>      ;WReg=WF
RM         PHI,     <WA,WPHI>    ;Areg=PHIreg=PHI
RM         DPHI,    <WB>        ;Breg=DPHI
RADD       PHI,     <WB>        ;PHI=PHI+DPHI
RM         WF,      <WB,WA,WSP> ;Breg=WF, A set to 0 if no carry or
           ;WF=finalWF, A set to 100H otherwise.
           ;Clrqt set if carry and WF=finalWF and
           ;end=1. INTMOD set.
RADD       WF,      <WB,clearB> ;Breg=0, WF=WF+0 or WF+1
RADD       AMP,     <WB,WSP>    ;AMP=0 and interrupt request if WF=finalWF
           ;and end=1
RM         AMP,     <WB,WSP>    ;X=mem(WF,PHI) Y=AMP mix update
RSP        ;wait multiply
RSP        ;wait multiply
RSP        ;accumulate
FIN

```

8-5-2 One-shot wave-form period

It is often necessary to generate only one period or a portion of a wave-form period. This is useful for envelope generation, but also for synthesis like FOF, where the shape of the pattern generated should be independent of the repetition rate of the pattern. It is also useful for transients generation, like clicks, frequency transients, etc.

The next example shows the generation of a single sinus period ; an interrupt to the main computer will be generated at the end of the period if the interrupt mask is resetted.

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;initial phase set by main computer

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```

PHI=0
DPHI=1
AMP=2

RM      PHI,      <WA, WPHI, WSP>      ;Areg=PHIreg=PHI Clrrqst=1,INTMOD=0
;Wfreg=100N (sinus)
RM      DPHI,     <WB>                ;Wreg=DPHI
RADD    PHI,      <WM, WSP>           ;write to D-RAM only if carry=0, generate
;interrupt if carry=1
...

```

Next example shows the generation of a single sinus period, frequency defined by DPHI1, repeated at the rate DPHI2. Interrupts should be masked.

```

PHI1=0      ;phase of sinus
DPHI1=1     ;frequency of single period
AMP=2       ;amplitude and mix

PHI2=3      ;phase of repetition rate
DPHI2=4     ;repetition rate
K=5         ;constant set at 40000N by computer (end=1, Wf=finalWf=0)

RM      PHI2,     <WA>                ;Areg=PHI2
RM      DPHI2,    <WB>                ;Wreg=DPHI2
RADD    PHI2,     <WM>                ;PHI2=PHI2+DPHI2
RM      K,        <WA, clearB, WSP>   ;Areg=Wreg=0 clrrqst=1 if cy=1
RADD    PHI1,     <WM, WSP>           ;clear PHI1 if clrrqst (once every period)
;of PHI2)

; one shot period
RM      PHI1,     <WA, WPHI, WSP>     ;Areg=PHIreg=PHI1 Clrrqst=1
;Wfreg=100N (sinus)
RM      DPHI1,    <WB>                ;Wreg=DPHI1
RADD    PHI1,     <WM, WSP>           ;write to D-RAM only if carry=0
RM      AMP,      <WXY, WSP>         ;X=sin(PHI1) Y=amp mix update

RSP      , <WACC>
FIN

```

More examples can be found in the algorithm library (SAM toolkit)

2- Writing to an external RAM sampling memory

There is no direct way for the main computer to read or write from/to an external memory connected to the SAM. However, defining an algorithm which will read the external memory in a block basis into the D-RAM is easy, and the computer can then read the D-RAM.

Writing data to an external RAM is done also with a specific algorithm, but specific micro-instructions are needed to control the memory signals as follows :

```

PHI=0      ;lower part of memory address (upper 9 bits)
WF=1       ;0(2)WF(8)X(9) upper part of memory address
DATA=2     ;data to be written in memory

RM      WF,       <WAF>                ;activate memory chip select (WCS/)
RM      PHI,      <WPHI>               ;PHIreg=PHI
RM      DATA,    <WXY>               ;prepare to output data on WD pins
RSP      ,        <ClearB, WSP>        ;WOE/=1 (disable outputs from external mem)
RSP      ,        <ClearB, WSP>        ;WOE/=1, apply data to WD pins
RSP      ,        <ClearB>             ;WOE/=1 WOE/=0 (write pulse)
RSP      ,        <ClearB>             ;WOE/=1 WOE/=0
RSP      ,        <ClearB, WSP>        ;WOE/=1 WOE/=1 data still applied
;data removed
;WOE/=0 (back to normal operation)

```

The complete write cycle takes 443 ns. This algorithm can be improved to transfer several words and generate an interrupt at transfer end.

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10- SAM micro-processor interface10-1 Control byte

The control byte is write only. It is updated when a computer write occurs to the chip with A2=1.

Control byte format :

| X | X | X | X | X | SSR | IDL | SEL | WR |

SSR 0- Select 44.1 kHz sampling rate
 1- Select 22.05 kHz sampling rate

IDL 0- Normal operation
 1- Force all 16 slots to idle algorithm

SEL 0- Select access to D-RAM
 1- Select access to A-RAM

WR 0- Request a read from D-RAM or A-RAM
 1- Request a write to D-RAM or A-RAM

Note : When IDL is changed from 0 to 1, it takes up to 1.5 /us [3 /us] for the SAM to actually go into an idle state.

10-2 Address, data and interrupt bytes

A write to the chip with A2=A1=A0=0 selects the internal RAM address

| V3 | V2 | V1 | V0 | MAD3 | MAD2 | MAD1 | MAD0 | D-RAM

| AL2 | AL1 | AL0 | PC4 | PC3 | PC2 | PC1 | PC0 | A-RAM with SSR=0

| AL2 | AL1 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 | A-RAM with SSR=1

V : slot number
MAD: D-RAM address inside slot (MAD from micro-instruction)
AL : algorithm number
PC : micro-instruction location counter inside algorithm

Write or read to the chip with A2=0 and A1A0 <> 00 allows to write/read data to/from the internal RAMs as follows :

| X | X | X | X | X | X | A1=1 A0=1 | 818 | 817 | 816 | 815 | 814 | 813 | 812 | 811 | 810 | 89 | 88 | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 |

Write or read to D-RAM

| X | X | X | X | X | X | X | X | X | A1=1 A0=0 | 114 | 113 | 112 | 111 | 110 | 109 | 108 | 107 | 106 | 105 | 104 | 103 | 102 | 101 | 100 |

Write or read to A-RAM

B is the 19 bits word of the D-RAM, I is the 15 bits micro-instruction word of the A-RAM.

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10-3 Operation

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Warning : before writing to the A-RAM, to avoid transient sounds at the output, care must be taken that the corresponding algorithm is not active, which can be done by setting the SAM idle in the control byte or making sure that all slots that reference the algorithm are in the idle state.

10-3-1 Writing to the D-RAM or the A-RAM

- 1- Write address
- 2- Write data
- 3- Write control byte with WR=1
- 4- Allow 1.5 /us [3 /us] recovery time for the write to perform

Notes :

The data bytes will retain their value from one write to another, which means that to write repetitive data, the write data step can be omitted.
Step 4 can be omitted if the SAM is in the idle state in the control byte

10-3-2 Reading the D-RAM or the A-RAM

- 1- Write address
- 2- Write control byte with WR=0
- 3- Wait 1.5 /us [3 /us] for the read to perform
- 4- Read the data bytes

Notes:

X portions of the data bytes will give indeterminate results
Step 3 can be omitted if the SAM was in the idle state in the control byte

10-4 Interrupt byte

The WM WSP micro-instruction can generate an interrupt (see §8-4). The processor can then read which memory location of the D-RAM caused the interrupt by reading the SAM with A2=A1=A0=0.

V3	V2	V1	V0	MAD3	MAD2	MAD1	MAD0	D-RAM
----	----	----	----	------	------	------	------	-------

This will not reset the interrupt cause. The interrupt cause can be removed by changing the corresponding slot parameters in the D-RAM or masking the interrupt of the corresponding slot (address V[15]).

In any case, once the interrupt cause has been removed, a dummy read interrupt should be issued to remove a possible pending interrupt with the same cause :

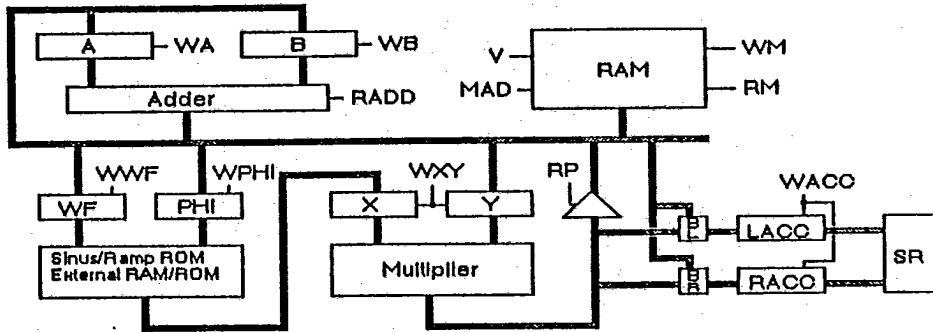
- 1- read interrupt byte
- 2- remove interrupt cause
- 3- read interrupt byte and discard result

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Figure 1 : SAM simplified diagram (data path)

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19 bits emitters : D-RAM (RM), Adder (RADD), Multiplier (RP)
 19 bits receivers : D-RAM (WM), Areg (WA), Breg (WB)
 12 bits receivers : PHireg (WPHI), Yreg (WXY)
 9 bits receiver : WFreq(WWF)
 3 bits receivers : BL and BR, right and left attenuators (WXY WSP)

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Appendix I - Sinus, ramps and constants specifications

"PHI" relates to the 12 upper bits of the phase considered as an unsigned integer (0 to 4095)

"X" relates to the corresponding input of the multiplier, considered as a fractionnal number between -1 and 1-2⁻¹¹.

Then the sinus is defined as :

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$$X = .71875 \sin \left(\left(\frac{PI}{2048} \right) \times PHI + \frac{PI}{4096} \right)$$

The ramp "PHI" is defined as :

$$X = \frac{PHI}{2048} \quad 0 \leq PHI < 2048$$

$$X = \frac{PHI}{2048} - 2 \quad 2048 \leq PHI < 4095$$

The ramp "2 x PHI" is defined as :

$$X = \frac{PHI}{1024} \quad 0 \leq PHI < 1024$$

$$X = \frac{PHI}{1024} - 2 \quad 1024 \leq PHI < 3072$$

$$X = \frac{PHI}{1024} - 4 \quad 3072 \leq PHI < 4095$$

The ramp "PHI/2" is defined as :

$$X = \frac{PHI}{4096} \quad 0 \leq PHI < 2048$$

$$X = \frac{PHI}{4096} - 1 \quad 2048 \leq PHI < 4095$$

The constants are derived from the MAD part of the micro-instruction, as defined in the corresponding fields of RM(MAD), WM(MAD), AD(MAD) as follows :

MAD	corresponding X value
0000	.0004883
0001	.06299
0010	.12549
0011	.18799
0100	.25049
0101	.31299
0110	.37549
0111	.43799
1000	.50049
1001	.56299
1010	.62549
1011	.68799
1100	.75049
1101	.81299
1110	.87549
1111	.93799

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Appendix II - Summary of Instructions and D-RAM formats

Emitters:

RM : put the content of D-RAM [MAD] on the bus
RADD : put the result of the adder on the bus
RP : put the result of the multiplier on the bus
RSP : nop, put nothing on the bus

Receivers:

WA : write the bus to A (19 bits).WA (without WSP) always sets the internals CLEARRQST flip-flop and clears the INTMOD flip-flop.
WB : write the bus to B (19 bits)
WM : write the bus to D-RAM[MAD]
WWF : write the bus to WF (9 bits, B9-B17)
WPHI : write the bus to PHI (12 leftmost bits, B7-B18)
WXY : write the bus to Y (12 leftmost bits),write the WF data to X

modifier:

WSP : modifier used in combination with WPHI,WXY,WA,WM
WPHI WSP : PHI loaded but-WF forced to 1 (select internal sinus).
WPHI WSP takes priority other WA WSP giving a normal WA
WXY XSP : Y and MIX loaded
WA WSP : expects an E[WAVE]final[WAVE] format on the bus (see §4)

WSP	CARRY	WF=finalWF	END	value loaded in A	CLEARRQST	INTMOD
no	X	X	X	19 bits bus	1	0
yes	0	X	X	00000H	0	1
yes	1	no	X	00200H	0	1
yes	1	yes	0	00000H	0	1
yes	1	yes	1	00000H	1	1

WM WSP :This micro-instruction allows to conditionally write to the D-RAM, according to CLEARRQST and CARRY. Also, an interrupt may be requested to the external processor, assuming that the interrupt mask bit at D-RAM address 15 is reset (see §4).

CLEARRQST	CARRY	INTMOD	write bus to D-RAM	Request Interrupt
no	X	X	no	no
yes	0	0	yes	no
yes	0	1	yes	yes
yes	1	X	no	yes

special actions:

clearB : write 0 in B , used also to write in external memory
WACC : send the multiplier result to final accumulator

DRAM-Formats:

18	10	7	0
PHI			
PHIWF		X	
PHIREG		X	
DPHI			
AMP		IX MIXL MIXR	
WAVE		FINAL WAVE	
[0] ext mem wave			
[1] R1 SELIZ		X	
X		[1] ALG [1] X	

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Appendix III - Micro-Instruction coding

114	113	112	111	110	109	108	107	106	105	104	103	102	101	100
MAD						WSP	WA	WB	WM	WPH	WXY	clear P	WJF	WACC
				00- RM										
				01- RADD										
				10- RP										
				11- RSP										

All Wxx and clearP are active 0 except WSP

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